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(54) Method and apparatus for providing the lock of a phase-locked loop system to a frequency sweep

Verfahren und Einrichtung zur Verriegelung eines Phasenregelkreises mit einer Ablenkfrequenz

Procédé et dispositif pour verrouiller une boucle à verrouillage de phase à une fréquence de balayage

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Description

This invention relates to improvements in methods for providing a smooth transition from open-loop step-up of a system frequency to closed-loop phase-locked loop (PLL) control by synchronization of the voltage-controlled oscillator (VCO) when the open-loop frequency is within pull-in range, and to circuits for accomplishing the same.

Although the present invention pertains to voltage controlled oscillator (VCO) synchronization of phase-locked loop (PLL) systems in general, it finds particular application in conjunction with polyphase DC motors, particularly of the brushless, sensorless, three-phase type used for rotating data media, such as are found in computer-related applications, such as hard disc drives, CD ROM drives, floppy disc drives, and the like. In such computer applications, three-phase, brushless, sensorless DC motors are becoming more popular, due to their reliability, low weight, and accuracy.

Brushless DC motors are commonly driven by a speed-controller that utilizes two functional loops: an overall speed-control loop, typically a PLL circuit, and a phase switching loop. A typical prior art motor speed-controller 10 is shown in Figure 1. The outer speed control loop 13 has a phase comparator 11 that compares a reference frequency, F_{REF}, applied to an input line 14 with a signal developed by a signal processor 20 from the stator windings of a motor 19. The phase difference signal developed by the phase comparator 11 is filtered by a filter 12 to drive switch logic circuitry 15, which in turn drives the motor 19 via appropriate drive circuitry 16. The outer speed control loop 13 ensures that the desired motor speed, set by the reference frequency, F_{REF}, on a line 14, is maintained. The phase switching inner loop 17 generates a timing signal that is sent to the switch logic circuit 15 to time the commutations in the stator coils 21 that drive the motor 19. In order to properly time the commutations in the circuit 10, however, the exact position of the rotor 18 must be determined. In the past, sensors, such as Hall or optical sensors, have been used to determine the position of the rotor. A more recent approach uses back emf information derived from selected ones of the stator coils 21 of the motor 19 to determine the location of the rotor 18. In such approach, as the magnetic rotor 18 passes a "floating" stator coil, it acts as a generator in regard to the coil and impresses an electromotive force or "back emf" on the coil. The back emf signal is processed and routed to the switching logic system to obtain the correct phase-switching. The back emf detection information not only enables the position of the rotor 18 to be determined, but the speed of the motor 21, as well. This motor speed information is fed back to the phase-comparator 11 of the outer speed-control loop 13 to maintain the desired motor operating speed.

US Patent No. 4673849 discloses a closed-loop drive system for a permanent magnet motor wherein in normal operation a sensing coil provides a back emf signal which is used to control the drive to the motor, the back emf signal also controlling the commutation of the motor switching devices.

The inner phase-switching loop 17 can be implemented in several ways. As mentioned, the clock signal for phase-switching in the inner loop may be provided by filtering the back emf of the motor 19 and extracting timing information with a signal processor 20. This involves determining the "zero-crossing" of the back emf, and using delays to control the timing of the switching.

US Patent No 4743815 discloses a control system for a multiphase brushless permanent magnet motor which operates in closed loop mode during normal operation. A microprocessor is responsive to a signal from a zero-crossing detector to commutate the switching devices of the motor, thereby controlling the timing of the commutation. During start-up the motor operates in open-loop, the switch-over from open-loop to closed loop being controlled by the microprocessor.

A more sophisticated approach shown in Figure 2 is similar to that of US patent 4,928,043, and uses a phase-locked loop (PLL) 35 to phase-track the back emf, in place of the signal processor 20. The phase-locked loop 35 includes a filter 32 connected to receive a signal derived from the back emf generated by the rotor 18 of the motor 19, to produce an output to a phase comparator 34. The phase comparator 34 compares the back emf signal with a desired phase signal (not shown) and produces an output to a second filter 36 to provide an error voltage to a voltage controlled oscillator (VCO) 38. In this approach, the back emf is used as an input to the PLL 35, and the output of the PLL 35 is fed to the phase-switching logic circuitry 15. In this way, the phase-switching logic circuitry 15 is synchronized to the back emf. This configuration offers better performance, since it reduces "phase-jitter", rapid, uncontrolled rotor movements due to imprecisely-timed phase-switching. The drawback of this approach is that at low motor speeds that occur when the motor 19 is first starting, the back emf signal is not of sufficient magnitude to drive the loop. In addition, as with any PLL loop, "lock" can be established in only a limited range of frequencies, and therefore during most of the start-up phase, the switching frequency is outside (lower than) the "lock" range. Thus, the motor 19 is generally ramped-up to speed open-loop, with the timing signal to the switching logic being provided by an external clock. The desired final operating state is a closed-loop mode in which the clock to the phase-switching is provided by a voltage-controlled oscillator (VCO) 38.

US Patent No. 4972442 discloses a closed-loop PLL, incorporating a voltage-controlled oscillator, in which a microprocessor controls the switching between a mode of operation in which the voltage controlled oscillator is driven by a near constant voltage signal such that a state of equilibration is maintained in the PLL, and a mode in which the PLL is locked to a reference signal.

What is needed is a way to produce a transition from open-loop operation to closed-loop operation without significant error in the switching timing that makes the loop incapable of locking and which may consequently stall the motor.

It is, therefore, an object of the invention to provide an improved circuit and method to provide a smooth transition from open-loop step-up of a system frequency to closed-loop PLL operation by synchronization of a VCO to the open-loop frequency when that frequency is within pull-in range.

It is another object of the invention to provide an improved apparatus and method of the type described to be used for starting DC motors, particularly of the brushless, sensorless type that are used for rotating data media, such as are found in computer-related applications, including hard disc drives, CD ROM drives, floppy disc drives, and the like.

It is still another object of the invention to provide an improved apparatus and method of the type described that enables a smooth transition from open-loop motor operation to closed-loop operation without a significant error in the sequence of the switching timing that would make the loop incapable of locking and would stall the motor.

These and other objects, features and advantages of the invention will be apparent to those skilled in the art from the following detailed description of the invention, when read in conjunction with the accompanying drawings and appended claims.

According to the present invention there is provided a circuit for producing a drive signal for starting and operating a polyphase motor having a back emf in a floating coil, comprising a source providing an initial reference voltage (V_{REF}), a source of clock pulses (EXT CLK) of successively decreasing periods, a voltage controlled oscillator having an input for receiving an input voltage and having a VCO output, said voltage controlled oscillator having a resynchronizing input for reinitiating said VCO output on each clock pulse of said source of clock pulses (EXT CLK), a period comparator for comparing the period of said clock pulses (EXT CLK) to the period of said VCO output, a phase comparator for comparing the phases of the back emf and said VCO output, first, second, and third switches controlled by said period comparator, said first switch for switching the input of said voltage controlled oscillator from said initial reference voltage (V_{REF}) to said output of the phase comparator when the period of said clock pulses becomes less than the period of said VCO output, said second switch for switching from said clock pulses (EXT CLK) to said VCO output to provide said drive signal when the period of said clock pulses (EXT CLK) becomes less than the period of said VCO output and said third switch for disabling said resynchronizing input from said clock pulses when the period of said clock signal (EXT CLK) becomes less than the period of said VCO output.

The invention provides a method according to Claim 11 of synchronizing a phase-locked loop to external pulses of successively decreasing period. In accordance to the method, a VCO of the phase-locked loop is operated to generate a plurality of pulses having a reference period. The pulses of the VCO are synchronized to the external pulses until the period of the external pulses are less than the reference period, and when the period of the external pulses becomes equal to the reference period, the phase-locked loop is switched to control the VCO.

The external pulses are directed to an output to drive a load until the period of the external pulses becomes equal to the reference period, and thereafter the output of the VCO of the phase-locked loop is provided. In addition, a status signal is generated in response to a condition of the load, and a phase difference is determined between the status signal and the VCO. The phase-locked loop is then operated in accordance with the phase difference. The status signal can be generated from a signal from a back emf of a floating coil of a polyphase motor that indicates the position of a rotor of the motor, and the signal from a back emf of a floating coil can be used as an input to the phase-locked loop.

The invention is illustrated in the accompanying drawings, in which:

Figure 1 is an electrical block diagram of a typical prior art motor speed control system, incorporating an outer motor speed-control loop and an inner phase-switching loop.

Figure 2 is an electrical block diagram of a typical prior art motor speed control system, incorporating an outer motor speed-control loop and an inner loop for phase-switching that utilizes a PLL circuit.

Figure 3 is an electrical block diagram of an inner loop for phase-switching in a motor driving system incorporating a motor starter system incorporating a VCO synchronization system in accordance with a preferred embodiment of the invention. The arrow notations in the switches indicate the change from open-loop mode to closed-loop mode.

Figure 4 is an electrical schematic diagram of a preferred embodiment of the period comparator shown in Figure 3.

In the various figures of the drawing, like reference numerals are used to denote like or similar parts.

The invention has many applications, particularly in motor controllers where the initial ramp-up of the motor speed is obtained in an open-loop configuration but the final speed of the motor is controlled by a PLL circuit. As noted previously motor-controllers of the prior art include the general idea of using an overall speed-control loop and an inner phase-switching loop. The prior art also includes the use of filtered back emf as a basis for phase-switching in the inner loop and the use of a PLL in the inner-loop to synchronize the switching clock to the back emf signal. The inner phase-switching loop is the part of the system wherein the subject invention is

implemented.

In contrast, an electrical schematic block diagram of an inner phase-switching loop 40 in which the apparatus and method in accordance with a preferred embodiment of the invention may be incorporated is shown in Figure 3. Although the switching loop 40 can be constructed of discrete components, preferably the circuit is integrated onto a single semiconductor chip (denoted by the dotted line 41) adapted for connection into an overall motor-starting and speed-control system.

As noted before, this system achieves a smooth transition between the open-loop motor-starting phase and closed-loop control. When the system is started, the open-loop phase begins during which the motor switching clock 64 is supplied by an external clock, EXT CLK, on a line 58 via a switch 60. The EXT CLK signal on the line 58 begins at zero frequency and is gradually increased in a linear fashion so as to not quickly escape the capture-range of the VCO 52 before it can be locked-onto. This slow ramp-up is also necessary because motors have a limited capability for acceleration. Also, at the beginning, the reference voltage (V_{REF}) applied to a line 46 is placed on the input to the voltage-controlled oscillator (VCO) 52. V_{REF} is the voltage necessary to set the output of the VCO 52 at the "switch over" frequency preselected by the user to be within the pull-in range of the PLL system. By way of example, the switches 48, 54, and 60 discussed above may be realized by any number of devices including mechanical switching devices and multiplexers implemented on integrated-circuit devices. Similarly, the VCO 52 may be realized by any number of devices, including properly setup 555-timer integrated-circuits or any of several different analog implementations.

The filter 50 is preferably a proportional integral filter, in order to minimize phase error. Since an integrating filter is used, the integrating capacitor must be maintained discharged so as to know exactly the output voltage. Such a clamping may be effected within the filter itself.

As mentioned previously, the VCO 52 is part of the PLL system 40 and will provide the motor switching clock signal on the line 64 after the switch over point is reached. During the open-loop startup phase of operation, the switch 54 assists in synchronizing the VCO 52 to the EXT CLK signal on the line 58 by routing the EXT CLK signal pulses via line 53 to the SYNC input of the VCO 52 to cause the output of the VCO 52 to restart on each pulse of the EXT CLK signal. The restarting of the VCO 52, for example, can be achieved in a manner similar to the reset function provided on a standard 555 timer chip, and serves to synchronize the output of the VCO 52 with the EXT CLK signal, enabling smooth transition on switch over after startup as described below.

The EXT CLK signal also goes to the switch logic via the switch 60 and to the period comparator 62 so that its period may be compared to the period of the VCO 52 output that was set at the switch over frequency. When the EXT CLK signal to the motor 19 reaches a lower period (i.e., higher frequency) than the VCO 52 output frequency, the switch over will occur. At that point the period comparator 62 will trigger the switch over to closed-loop mode by signaling switch 54 to switch the synchronizing input of the VCO 52 from the EXT CLK signal to a reference potential 56, typically ground, by signaling the switch 48 to switch the input of the VCO 52 from V_{REF} on line 46 to the output of the phase comparator 44, and by switching the output of the phase-switching loop 40 (i.e., input to the switching logic) from the EXT CLK signal to the output of the VCO 52. By switching the SYNC input from the EXT CLK signal to the reference potential, the synchronizing of the VCO 52 to the EXT CLK signal is halted, to enable the VCO 52 to run at the desired final speed. In closed-loop operation, the back emf signal on the line 42 from the motor 19 is compared with the output of the VCO 52 by the phase comparator 44. This speeds up the output of the VCO 52 when a phase difference occurs between the back emf on the line 42 and the VCO 52 output. In this fashion, the PLL loop produces a motor switching clock signal on the line 64 that tracks the back emf signal on the line 42.

Thus, a smooth transition to closed-loop operation is achieved. This phase-switching circuit 40 minimizes "jolt" in the motor 19 because the frequency and phase of the VCO 52 is synchronized to the exterior clock signal on line 58. This is important because if the first pulse from the VCO 52 after the switch over is out of phase or is not frequency synchronized with the preceding EXT CLK pulse then the lock on the motor 19 will be lost.

Thus, demanding phase and frequency requirements are placed on this type of circuit. In other applications, if the VCO is inserted with a phase error, the loop will adjust with time. However, in a motor application if the lock is missed the motor 19 must be slowed down to zero speed and restarted. It will be appreciated that acquiring lock-on may be difficult if a phase error is introduced due to motor inertia and erroneous torque generation. It is therefore desirable to get a correct phase-lock-on the first time, as achieved by the phase-switching circuit 40.

The period comparator 62 may be implemented by any number of "off the shelf" devices, including integrated-circuits that have been specially designed for comparing the period of various signals and that are widely available for such applications. Figure 4 is a block diagram of one particular embodiment of the period comparator 62 that is shown in Figure 3. This device utilizes three D-type flip-flops 72, 76, and 78, and waits for two consecutive positive edges of pulses from the EXT CLK 58 to occur before a second positive edge of a VCO 52 pulse occurs to determine whether the frequency of the EXT CLK signal has exceeded the VCO 52 output frequency on a line 55. Since the VCO 52 will initially be oscillating faster than the EXT CLK signal the first pulse the period comparator 62 will receive will be from the

VCO 52.

Referring to Figure 4, the output from the VCO 52 will clock the first D flip-flop 72, causing a low state at its Q(bar) output. When a positive edge of an EXT CLK pulse occurs, it resets the first flip-flop 72 while simultaneously clocking the second flip-flop 76. Due to the propagation delay of the first flip-flop 72, the low state that was present at its Q(bar) output will be clocked into the D input of the second flip-flop 76 before the reset of the first flip-flop 72 occurs. Therefore, this low state will be clocked through the second flip-flop 76. Soon thereafter, the Q(bar) output of the first flip-flop 72 changes to a high state, since it was reset. If another positive edge of an EXT CLK pulse occurs before a positive edge of a pulse from the VCO 52 occurs, then the Q(bar) output of the first flip-flop 72 remains high because of the reset. This second EXT CLK pulse will clock a high state to the Q output of the second flip-flop 76. The falling edge of the EXT CLK pulse, inverted by the invertor 80, will clock the high state from the Q output of the second flip-flop 76 through the third flip-flop 78 to its Q output regardless of the state of the VCO output 55.

Thus, the circuit 62 looks for two positive pulse edges from the EXT CLK signal before the completion of a VCO 52 cycle (i.e., two adjacent positive pulse edges), and when this occurs signals the switches 48, 54, and 60 in the circuit 40 to change states as indicated by the arrows in Figure 3. It will be appreciated that the third flip-flop 78 is not strictly necessary to the determination of when the frequency of the EXT CLK signal exceeds the output frequency of said VCO 52 since the desired output was generated on the Q output of the second flip-flop 76 upon receipt of the second rising edge of the EXT CLK signal. In many implementations the phase-switching circuitry 40 will work without the third flip-flop 78, but in the implementation illustrated, the switch over signal is delayed by the length of the EXT CLK pulse signal to give a slower analog VCO 52 time to begin operation.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the scope of the invention, as hereinafter claimed.

The present invention may provide a circuit in which the switches are integrated-circuit devices.

Claims

1. A circuit for producing a drive signal for starting and operating a polyphase motor having a back emf (42) in a floating coil, comprising:

   a source providing an initial reference voltage (V_{REF});
   a source of clock pulses (EXT CLK) of successively decreasing periods;
   a voltage controlled oscillator (52) having an input for receiving an input voltage and having a VCO output, said voltage controlled oscillator (52) having a resynchronizing input (53) for reinitiating said VCO output on each clock pulse of said source of clock pulses (EXT CLK);
   a period comparator (62) for comparing the period of said clock pulses (EXT CLK) to the period of said VCO output;
   a phase comparator (44) for comparing the phases of the back emf (42) and said VCO output;
   first (48), second (60), and third (54) switches controlled by said period comparator;
   said first switch (48) for switching the input of said voltage controlled oscillator (52) from said initial reference voltage (V_{REF}) to said output of the phase comparator (44) when the period of said clock pulses becomes less than the period of said VCO (52) output;
   said second switch (60) for switching from said clock pulses (EXT CLK) to said VCO (52) output to provide said drive signal when the period of said clock pulses (EXT CLK) becomes less than the period of said VCO (52) output; and
   said third switch (54) for disabling said resynchronizing input (53) from said clock pulses when the period of said clock signal (EXT CLK) becomes less than the period of said VCO (52) output.

2. The circuit of claim 1 wherein said period comparator (62) comprises flip-flop circuits (72,76,78) to compare a positive edge of a pulse from said voltage controlled oscillator (52) with a positive edge of said clock pulses.

3. The circuit of claim 2 wherein said flip-flop circuits (72,76,78) operate to switch said first (48), second (60), and third (54) switches when two positive edges of the clock pulses occur before a second positive edge from said voltage controlled oscillator (52) occurs.

4. The circuit of claim 2 or claim 3 wherein said flip-flop circuits (72,76,78) are D-type flip-flops circuits.

5. The circuit of claim 3 wherein said period comparator (62) comprises:

   a first D-type flip-flop (72) having a D input (D), a clock input (CLK), a SET control input (S), a RESET control input (R), a Q output (Q), and a Q(bar) output (Q), wherein the D input has a reference potential (V_{CC}) impressed on it, the clock input is connected to the output frequency

of the voltage controlled oscillator (52), the SET control input is connected to an initializing control line, and the RESET control input is connected to said source of clock pulses;
a second D-type flip-flop (76) having a D input (D), a clock input (CLK), a RESET control input (R), a Q output (Q), and a Q(bar) output (Q), wherein the D input is connected to the Q(bar) output of the first D-type flip-flop (22), the clock input is connected to said source of clock pulses, and the RESET control input is connected to said initializing control line;
a third D-type flip-flop (78) having a D input (D), a clock input (CK), a RESET control input (R) a Q output (Q), and a Q(bar) output (Q), wherein the D input is connected to the Q output of the second D-type flip-flop (76), the RESET is connected to the initializing control line, and the Q output is connected to said first (48), second (60), and third (54) switches; and
an invertor (80) having an input connected to the source of clock pulses (EXT CLK) and an output connected to the clock input (CK) of said third D-type flip-flop (78).

6. The circuit of any one of claims 1 to 5 wherein said switches (48,60,54) are multiplexers.

7. The circuit of any of claims 1 to 6 wherein said switches (48,60,54) are integrated circuit devices.

8. The circuit of any one of claims 1 to 7 further comprising a filter (50) connected to an input of said voltage controlled oscillator (52) for reducing noise and circuit overshoot.

9. The circuit of claim 8 wherein said filter (50) is a proportional-type integral filter.

10. The circuit of any preceding claim wherein the entire circuit is integrated as a single integrated-circuit device.

11. A method of synchronizing a phase-locked loop to external pulses of successively decreasing period (EXT CLK), comprising:

operating a VCO (52) of the phase-locked loop to generate a plurality of pulses having a reference period,
synchronizing the pulses of said VCO to the external pulses until the period of said external pulses are less than said reference period;
determining when a period of said external pulses becomes equal to the reference period;
switching said phase-locked loop to control said VCO when the period of the external pulses becomes equal to the reference period.

12. The method of synchronizing a phase-locked loop of claim 11 further comprising:

directing said external pulses to an output until said period of said external pulses becomes equal to the reference period, and thereafter, providing the output of said phase-locked loop to drive a load.

13. The method of synchronizing a phase-locked loop of claim 12 further comprising:

generating a status signal (BEMF) in response to a condition of said load;
determining a phase difference between said status signal and said VCO;
and operating said phase-locked loop to operate in accordance with said phase difference.

14. The method of synchronizing a phase-locked loop of claim 13 wherein said step of generating a status signal in response to a condition of said load comprises generating a signal from a back emf of a floating coil of a polyphase motor that indicates the position of a rotor of the motor.

15. The method of synchronizing a phase-locked loop of claim 14 further comprising using said signal from a back emf of a floating coil as an input to said phase-locked loop.

Patentansprüche

1. Schaltung zur Erzeugung eines Treibersignals zum Starten und Betreiben eines vielphasigen Motors, der eine Rückwärts-EMK (42) in einer potentialfreien bzw. erdfreien Spule bzw. Wicklung hat, die aufweist:

eine Quelle, die eine anfängliche Bezugsspannung (V_{REF}) bereitstellt;
eine Quelle für Taktpulse (EXT CLK) mit aufeinanderfolgend abnehmenden Perioden;
einem spannungsgesteuerten Oszillator (52), der einen Eingang zum Empfangen einer Eingangsspannung hat, und der einen VCO-Ausgang hat, wobei der spannungsgesteuerte Oszillator (52) einen Resynchronisationseingang (53) hat, um den VCO-Ausgang bei jedem Taktpuls der Quelle der Taktpulse (EXT CLK) zu reinitiieren bzw. neu zu initiieren;
einen Periodenkomparator (62), um die Periode der Taktpulse (EXT CLK) mit der Periode des VCO-Ausgangs zu vergleichen;
einen Phasenkomparator (44), um die Phasen des Rückwärts-EMK (42) und des VCO-Ausgangs zu vergleichen;

einen ersten (48), einen zweiten (60) und einen dritten (54) Schalter, die durch den Periodenkomparator gesteuert werden;
der erste Schalter (48) ist zum Schalten des Eingangs des spannungsgesteuerten Oszillators (52) von der Anfangsbezugsspannung (V_{REF}) auf den Ausgang des Phasenkomparators (44), wenn die Periode der Taktpulse geringer wird als die Periode des Ausgangs des VCO (52);
der zweite Schalter (60) ist zum Schalten der Taktpulse (EXT CLK) auf den Ausgang des VCO (52), um das Antriebssignal bereitzustellen, wenn die Periode der Taktpulse (EXT CLK) geringer als die Periode des Ausgangs des VCO (52) wird; und
der dritte Schalter (54) ist zum Sperren des Resynchronisationseinganges von den Taktpulsen, wenn die Periode des Taktsignals (EXT CLK) geringer als die Periode des Ausgangs des VCO (52) wird.

2. Schaltung nach Anspruch 1, in der der Periodenkomparator (62) Flip-Flop-Schaltungen (72, 76, 78) aufweist, um eine positive Flanke eines Pulses von dem spannungsgesteuerten Oszillator (52) mit einer positiven Flanke der Taktpulse zu vergleichen.

3. Schaltung nach Anspruch 2, in der die Flip-Flop-Schaltungen (72, 76, 78) arbeiten, um den ersten (48), den zweiten (60) und den dritten (54) Schalter zu betreiben, wenn zwei positive Flanken der Taktpulse auftreten, bevor eine zweite positive Flanke von dem spannungsgesteuerten Oszillator (52) auftritt.

4. Schaltung nach Anspruch 2 oder Anspruch 3, in der die Flip-Flop-Schaltungen (72, 76, 78) Schaltungen von D-Typ-Flip-Flops sind.

5. Schaltung nach Anspruch 3, in der der Periodenkomparator (62) aufweist:

einen ersten D-Typ-Flip-Flop (72), der einen D-Eingang (D), einen Takteingang (CLK), einen Einstell-Steuereingang (S), einen Rücksetz-Steuereingang (R), einen Q-Ausgang (Q) und einen Q(Strich)-Ausgang (Q) hat, in dem der Eingang D ein Bezugspotential (V_{CC}), das diesem innewohnt, hat, wobei der Takteingang an die Ausgangsfrequenz des spannungsgesteuerten Oszillators (52) angeschlossen ist, wobei der Einstellsteuereingang an eine Initialisierungssteuerleitung angeschlossen ist und der Rücksetz-Steuereingang an die Quelle der Taktpulse angeschlossen ist;
einen zweiten D-Typ-Flip-Flop (76), der einen D-Eingang (D), einen Takteingang (CLK), einen Rücksetz-Steuereingang (R), einen Q-Ausgang (Q) und einen Q(Strich)-Ausgang (Q) hat, in dem der D-Eingang an den Q(Strich)-Ausgang des ersten D-Typ-Flip-Flops (22) angeschlossen ist, der Takteingang an die Quelle der Taktpulse angeschlossen ist und der Rücksetz-Steuereingang an die Initialisierungs- bzw. Auslösesteuerleitung angeschlossen ist;
einen dritten D-Typ-Flip-Flop (78), der einen D-Eingang (D), einen Takteingang (CK), einen Rücksetz-Steuereingang (R), einen Q-Ausgang (Q) und einen Q(Strich)-Ausgang (Q) hat, in dem der D-Eingang an den Q-Ausgang des zweiten D-Typ-Flip-Flops (76) angeschlossen ist, wobei die Rücksetzung an die Initialisierungs- bzw. Auslösesteuerleitung angeschlossen ist, und der Q-Ausgang an den ersten (48), den zweiten (60) und den dritten (54) Schalter angeschlossen ist; und
einen Inverter (80), der einen Eingang, der an die Quelle der Taktpulse (EXT CLK) angeschlossen ist, und einen Ausgang hat, der an den Takteingang (CK) des dritten D-Typ-Flip-Flops (78) angeschlossen ist.

6. Schaltung nach irgendeinem der Ansprüche 1 bis 5, in der die Schalter (48, 60, 54) Multiplexer sind.

7. Schaltung nach irgendeinem der Ansprüche 1 bis 6, in der die Schalter (48, 60, 54) integrierte Schalteinrichtungen sind.

8. Schaltung nach irgendeinem der Ansprüche 1 bis 7, die ferner einen Filter (50) aufweist, der an einen Eingang des spannungsgesteuerten Oszillators (52) angeschlossen ist, um Störungen bzw. Rauschen und ein Schaltungsüberschwingen zu verringern.

9. Schaltung nach Anspruch 8, in der der Filter (50) ein Integralfilter vom Proportional-Typ ist.

10. Schaltung nach einem der voranstehenden Ansprüche, in der die gesamte Schaltung als eine einzige integrierte Schaltungseinrichtung integriert ist.

11. Verfahren zum Synchronisieren einer phasenstarren Schleife an externe Pulse mit aufeinanderfolgend abnehmender Periode (EXT CLK), das aufweist:

ein VCO (52) der phasenstarren bzw. -synchronisierten Schleife wird betrieben, um mehrere Pulse, die eine Bezugsperiode haben, zu erzeugen,
die Pulse des VCO werden auf die externen Pulse synchronisiert, bis die bzw. Periode der externen Pulse geringer ist, als die Bezugspe-

riode;
es wird bestimmt, wenn eine Periode des externen Pulses der Bezugsperiode gleich wird;
die phasenstarre Schleife wird geschaltet, um den VCO zu steuern, wenn die Periode der externen Pulse der Bezugsperiode gleich wird.

12. Verfahren zum Synchronisieren einer phasenstarren Schleife nach Anspruch 11, das ferner aufweist:

die externen Pulse werden zu einem Ausgang geleitet, bis die Periode der externen Pulse der Bezugsperiode gleich wird, und danach,
wird der Ausgang der phasenstarren Schleife bereitgestellt, um eine Last zu betreiben.

13. Verfahren zum Synchronisieren einer phasenstarren Schleife nach Anspruch 12, das ferner aufweist:

ein Status- bzw. Zustandssignal (BEMF) wird in Reaktion auf einen Zustand der Last erzeugt;
eine Phasendifferenz wird zwischen dem Zustands- bzw. Statussignal und dem VCO bestimmt;
die phasenstarre bzw. -synchronisierte Schleife wird betrieben, um in Übereinstimmung mit der Phasendifferenz zu arbeiten.

14. Verfahren zum Synchronisieren einer phasenstarren Schleife nach Anspruch 13, bei dem der Schritt zum Erzeugen eines Zustands bzw. Statussignals in Reaktion auf einen Zustand der Last aufweist, daß ein Signal von einer Rückwärts-EMK einer potentialfreien bzw. erdfreien Spule bzw. Wicklung eines vielphasigen Motors erzeugt wird, daß die Stellung eines Rotors des Motors anzeigt.

15. Verfahren zum Synchronisieren einer phasenstarren Schleife nach Anspruch 14, das ferner aufweist, daß das Signal von einer Rückwärts-EMK einer potentialfreien bzw. erdfreien Spule bzw. Wicklung als ein Eingang zu der phasenstarren Schleife verwendet wird.

Revendications

1. Circuit pour produire un signal d'attaque pour démarrer et commander un moteur polyphasé ayant une force contre-électromotrice (42) dans une bobine flottante, comprenant :

une source délivrant une tension de référence initiale (V_{REF}) ;
une source d'impulsions d'horloge (EXT CLK) de périodes diminuant successivement ;
un oscillateur commandé en tension (52) ayant une entrée pour recevoir une tension d'entrée et ayant une sortie du VCO, ledit oscillateur commandé en tension (52) ayant une entrée de resynchronisation (53) pour relancer ladite sortie du VCO sur chaque impulsion d'horloge de ladite source d'impulsions d'horloge (EXT CLK) ;
un comparateur de période (62) pour comparer la période desdites impulsions d'horloge (EXT CLK) à la période de ladite sortie du VCO ;
un comparateur de phase (44) pour comparer les phases de la force contre-électromotrice (42) et de ladite sortie du VCO ;
des premier (48), deuxième (60) et troisième (54) commutateurs commandés par ledit comparateur de période ;
ledit premier commutateur (48) pour commuter l'entrée dudit oscillateur commandé en tension (52) provenant de ladite tension de référence initiale (V_{REF}) à ladite sortie du comparateur de phase (44) lorsque la période desdites impulsions d'horloge devient inférieure à la période de ladite sortie du VCO (52) ;
ledit deuxième commutateur (60) pour effectuer une commutation desdites impulsions d'horloge (EXT CLK) à ladite sortie du VCO (52) pour délivrer ledit signal d'attaque lorsque la période desdites impulsions d'horloge (EXT CLK) devient inférieure à la période de ladite sortie du VCO (52) ; et
ledit troisième commutateur (54) pour mettre hors service ladite entrée de resynchronisation (53) provenant desdites impulsions d'horloge lorsque la période dudit signal d'horloge (EXT CLK) devient inférieure à la période de ladite sortie du VCO (52).

2. Circuit selon la revendication 1, dans lequel ledit comparateur de période (62) comprend des bascules (72, 76, 78) pour comparer un front positif d'une impulsion provenant dudit oscillateur commandé en tension (52) avec un front positif desdites impulsions d'horloge.

3. Circuit selon la revendication 2, dans lequel lesdites bascules (72, 76, 78) fonctionnent pour commuter lesdits premier (48), deuxième (60) et troisième (54) commutateurs lorsque deux fronts positifs des impulsions d'horloge surviennent avant qu'un second front positif provenant dudit oscillateur commandé en tension (52) survienne.

4. Circuit selon la revendication 2 ou 3 dans lequel lesdites bascules (72, 76, 78) sont des bascules du type D.

5. Circuit selon la revendication 3 dans lequel ledit comparateur de période (62) comprend :

une première bascule du type D (72) ayant une entrée D (D), une entrée d'horloge (CLK), une entrée de commande de MISE A UN (S), une entrée de commande de REMISE A ZERO (R), une sortie Q (Q), et une sortie Q (barre) (Q), dans laquelle l'entrée D a un potentiel de référence (V_{CC}) qui lui est appliqué, dans laquelle l'entrée d'horloge est connectée à la fréquence de sortie de l'oscillateur commandé en tension (52), dans laquelle l'entrée de commande de MISE A UN est connectée à une ligne de commande d'initialisation, et dans laquelle l'entrée de commande de REMISE A ZERO est connectée à ladite source d'impulsions d'horloge ;
une deuxième bascule du type D (76) ayant une entrée D (D), une entrée d'horloge (CLK), une entrée de commande de REMISE A ZERO (R), une sortie Q (Q), et une sortie Q (barre) (Q), dans laquelle l'entrée D est connectée à la sortie Q (barre)
de la première bascule du type D (22), dans laquelle l'entrée d'horloge est connectée à ladite source d'impulsions d'horloge et dans laquelle l'entrée de commande de REMISE A ZERO est connectée à ladite ligne de commande d'initialisation ;
une troisième bascule du type D (78) ayant une entrée D (D), une entrée d'horloge (CK), une entrée de commande de REMISE A ZERO (R), une sortie Q (Q), et une sortie Q (barre) (Q), dans laquelle l'entrée D est connectée à la sortie Q de la deuxième bascule du type D (76), dans laquelle la REMISE A ZERO est connectée à la ligne de commande d'initialisation, et dans laquelle la sortie Q est connectée auxdits premier (48), deuxième (60) et troisième (54) commutateurs ; et
un inverseur (80) ayant une entrée connectée à la source d'impulsions d'horloge (EXT CLK) et une sortie connectée à l'entrée d'horloge (CK) de ladite troisième bascule du type D (78).

6. Circuit selon l'une quelconque des revendications 1 à 5, dans lequel lesdits commutateurs (48, 60, 54) sont des multiplexeurs.

7. Circuit selon l'une quelconque des revendications 1 à 6, dans lequel lesdits commutateurs (48, 60, 54) sont des dispositifs à circuit intégré.

8. Circuit selon l'une quelconque des revendications 1 à 7, comprenant en outre un filtre (50) connecté à une entrée dudit oscillateur commandé en tension (52) pour réduire du bruit et un dépassement positif de circuit.

9. Circuit selon la revendication 8, dans lequel ledit filtre (50) est un filtre intégral du type proportionnel.

10. Circuit selon l'une quelconque des revendications précédentes, dans lequel le circuit entier est intégré sous la forme d'un dispositif unique à circuit intégré.

11. Procédé de synchronisation d'une boucle à verrouillage de phase sur des impulsions externes de périodes diminuant successivement (EXT CLK), comprenant les étapes consistant à :

commander un VCO (52) de la boucle à verrouillage de phase pour produire plusieurs impulsions ayant une période de référence,
synchroniser les impulsions dudit VCO sur les impulsions externes jusqu'à ce que la période desdites impulsions externes soit inférieure à ladite période de référence ;
déterminer lorsqu'une période desdites impulsions externes devient égale à la période de référence ;
commuter ladite boucle à verrouillage de phase pour commander ledit VCO lorsque la période des impulsions externes devient égale à la période de référence.

12. Procédé de synchronisation d'une boucle à verrouillage de phase selon la revendication 11, comprenant en outre les étapes consistant à :

diriger lesdites impulsions externes vers une sortie jusqu'à ce que ladite période desdites impulsions externes devienne égale à la période de référence, et ensuite
délivrer la sortie de ladite boucle à verrouillage de phase pour commander une charge.

13. Procédé de synchronisation d'une boucle à verrouillage de phase selon la revendication 12 comprenant en outre les étapes consistant à :

produire un signal de statut (BEMF) en réponse à une condition de ladite charge ;
déterminer une différence de phase entre ledit signal de statut et ledit VCO ;
et commander ladite boucle à verrouillage de phase pour fonctionner en conformité avec ladite différence de phase.

14. Procédé de synchronisation d'une boucle à verrouillage de phase selon la revendication 13, dans lequel ladite étape de production d'un signal de statut en réponse à une condition de ladite charge comprend la production d'un signal depuis une force contre-électromotrice d'une bobine flottante d'un moteur polyphasé qui indique la position d'un rotor du moteur.

15. Procédé de synchronisation d'une boucle à verrouillage de phase selon la revendication 14, com-

prenant en outre l'utilisation dudit signal provenant d'une force contre-électromotrice d'une bobine flottante en tant qu'entrée vers ladite boucle à verrouillage de phase.

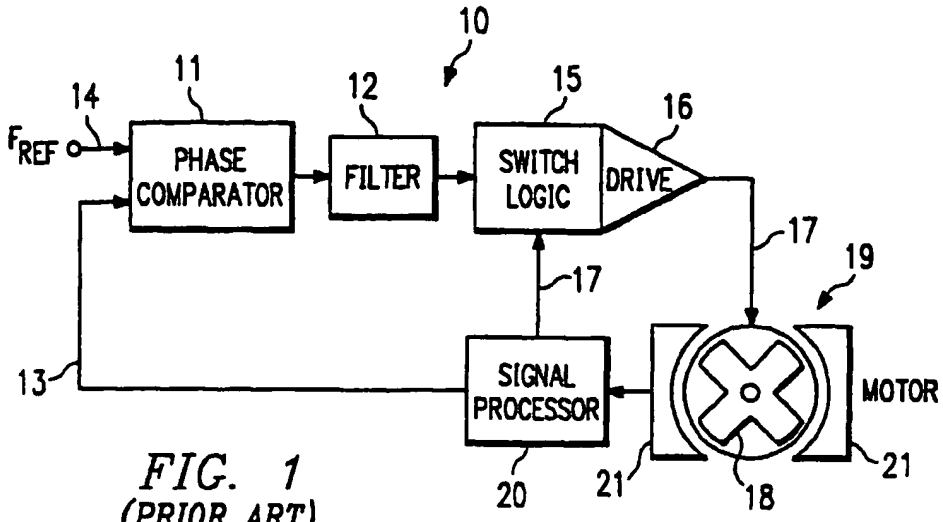

FIG. 1
(PRIOR ART)

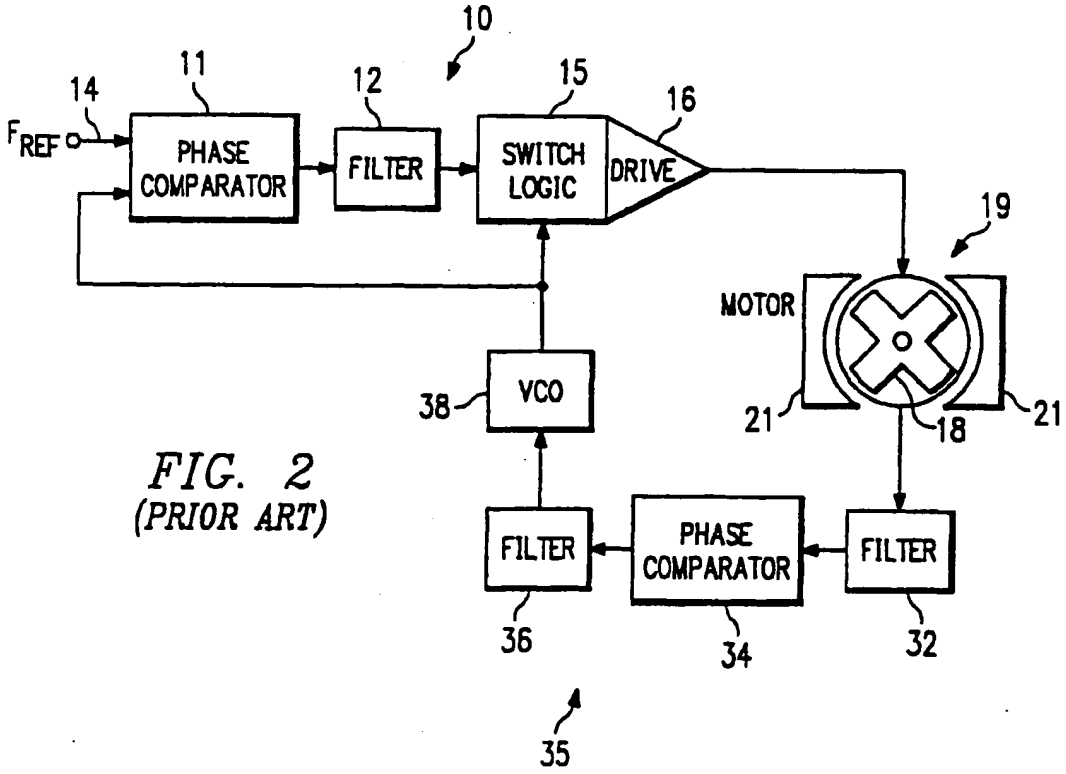

FIG. 2
(PRIOR ART)

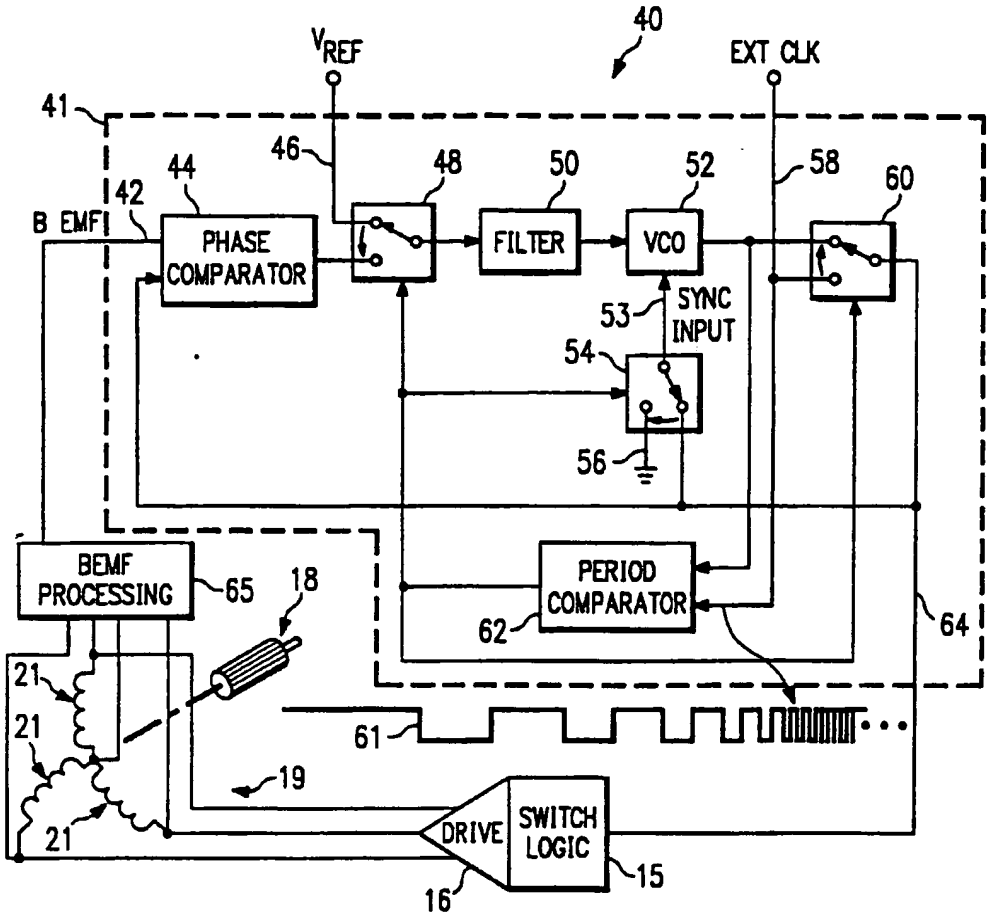
40
V_{REF}
EXT CLK
41
46
48
50
52
58
60
44
42
B EMF
PHASE COMPARATOR
FILTER
VCO
SYNC INPUT
53
54
56
BEMF PROCESSING
65
18
PERIOD COMPARATOR
62
64
21
21
21
61
19
DRIVE
SWITCH LOGIC
15
16

FIG. 3

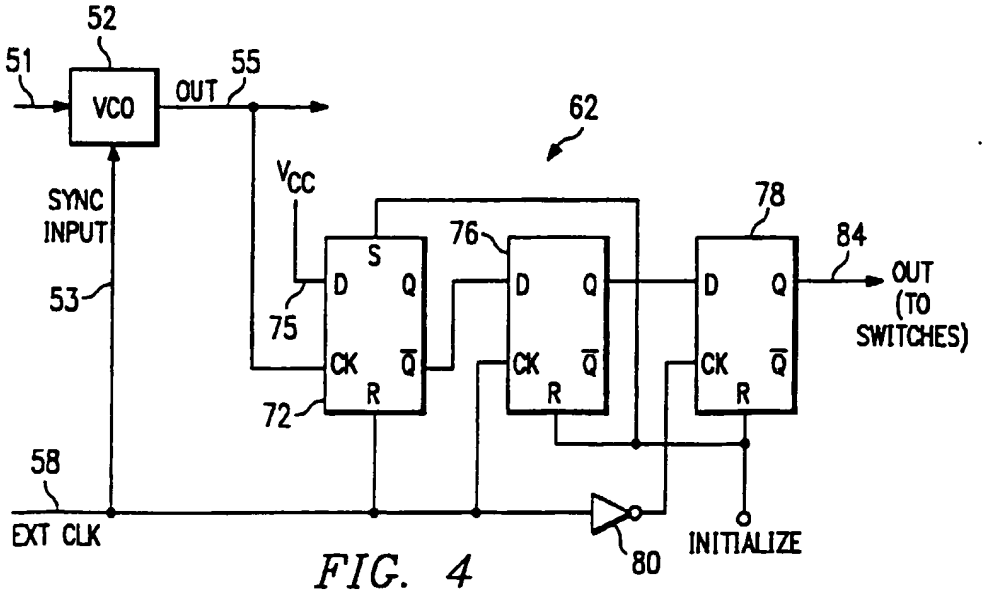
52
51
VCO
OUT
55
62
V_{CC}
SYNC INPUT
53
75
S
D
Q
CK
R
72
76
78
84
OUT (TO SWITCHES)
58
EXT CLK
80
INITIALIZE

FIG. 4